spacer means for protecting the electrode from a reoxidation, the spacer means comprising silicon nitride or an amorphous silicon film and being deposited on the sidewalls of the electrode and not on the first layer of oxide.

REMARKS

In response to the Office Action mailed January 11, 1999, the applicant requests reconsideration of the above-identified application in view of the following remarks. Claims 23-43 are pending in the application, and claims 23-43 are rejected. Claims 32-35 will be canceled and claims 23-26, 28-31, 36-40, 42, and 43 will be amended upon entry of the present amendment.

Telephone interview

The applicant thanks Examiner Nadav for the telephone interview granted on Thursday, February 25, 1999 between himself and the applicant's representative Mr. Mates (Reg. No.35,271).

Objection

The Examiner objected to claims 25, 29, 30, and 38. The applicant has amended the aforesaid claims to obviate the objection.

Drawings

The Examiner objected to the drawings. The applicant respectfully traverses. A layer of oxide is shown in each of Figures 2A-2D and this feature will be highlighted in the following remarks.

Rejections under 35 USC §112

Claims 23-31 and 36-43 are rejected under 35 USC § 112, first paragraph, because the terms "layer of gate oxide" and "first layer of oxide" are not supported by the specification. The applicant respectfully traverses.

The requirement for completeness of an application is set forth in MPEP 608.01(p): "A disclosure in an application, to be complete, must contain such description and details as to enable any person skilled in the art or science to which the invention pertains to make and use the invention as of its filing date." The applicant respectfully submits that a first layer of oxide, also called a layer of gate oxide, is shown in Figures 2A-2D and that its presence in Figures 2A-2D is amply supported by the specification and would be recognized and understood by those skilled in the art.

Figures 2A-2D show an electrode 205 over a layer 215 with a selective spacer 210 deposited only on the electrode 205 and not on the layer 215. The layer 215 is described as "active area 215" on page 4, line 27 and on page 5, lines 5-6. One skilled in the art will understand that the layer 215 is oxide, and that it happens to stretch between field oxide barriers over an "active area" at this particular stage in the fabrication of a CMOS device. The term "active area" is used to refer to the layer 215, and the rest of the specification clearly indicates to one skilled in the art that the layer 215 is oxide.

The term "active area" is well known to those skilled in the art. An "active area" of an integrated circuit is a two-dimensional area, looking down on a layout of the integrated circuit, in which a device such as a transistor is formed. The "active area" is the area of the integrated circuit between isolating regions of field oxide that are formed to electrically insulate neighboring devices from each other. The applicant has attached selections from two textbooks that disclose the meaning of the term "active area." The selections are attached for illustrative and teaching purposes only and need not be submitted in an Information Disclosure Statement under the exception described in MPEP §609 C(3).

The first selection is Neil H. E. Weste & Kamran Eshraghian, Principles of CMOS VLSI Design A Systems Perspective (1985), pages 71-72. A thin oxide or thinox mask is described as defining where areas of thin oxide are needed to implement devices. The term active area is given as another name for the mask, which is shown on page 72 having rectangular areas defining active areas for an integrated circuit.

The second selection is Lance A. Glasser & Daniel W. Dobberpuhl, The Design and Analysis of VLSI Circuits (1985), pages 4, 101-103, 176-179, 182, and 183. On page 4 the active area is described as including "regions of heavily doped single-crystal silicon and

B

transistor gate area". On page 102 the active area device edge is described as being moved by field oxidation. An "active area mask is used to define a region to be blocked from field oxidation." In other words, an active area mask defines active areas and insulating areas of field oxide. On page 103 it is stated that "[i]n MOS technology, oxide thickness is the primary parameter used to distinguish active (transistor) areas from inactive (field) areas." Here is a direct association between a layer of oxide and an active area of an integrated circuit, the active area being defined by a thickness of the layer of oxide. It is therefore not incorrect to point to a layer of oxide and call it an active area. An active area mask is mentioned again on page 176 as defining "what will eventually be sources, drains, channels, and diffused cross unders." The remaining pages describe and illustrate the role of the active area mask.

The focus of the description is on the selective spacer 210 which is deposited *only* on the electrode 205 and *not* on the layer 215 because of the phenomenon shown in Figure 1. Figure 1 illustrates that a "deposition of spacer materials on polysilicon 110 occurs more rapidly than deposition on oxide 120....The difference in incubation time 130 on dissimilar materials makes selective spacer deposition possible." Specification page 4, lines 8-12. Later it is stated that "Figures 2A-2D show how this incubation time difference 130 can be exploited for selective spacer deposition." Specification page 4, lines 19-20. With reference to the process: "In the second step, represented in Figures 2B and 2C, a selective spacer 210 is deposited such that the amount deposited on the polysilicon and refractory metal of electrode 205 is less than the incubation thickness, leaving the active area 215 free of deposition." Specification page 4, lines 24-27. Looking at Figure 2B one skilled in the art could only conclude that the layer 215 is oxide. The use of the term "active area" to describe the oxide layer 215 is not incorrect because the oxide covers the "active area" in which the CMOS device is being formed. As mentioned above, a thickness of the oxide layer 215 defines what is the active area. Proceeding with the description: "Once the spacer is deposited, the device undergoes polycide reoxidation 220....active area 215 and selective spacers 210 are reoxidized 220." Specification page 5, lines 3-6. The layer of reoxidation 220 shown in Figure 2C implies to one skilled in the art the existence of an original layer of oxide - the oxide layer 215.

The claims as filed also provide support for the oxide layer 215. In claim 9, line 3, the act of forming an *insulating layer* on a semiconductor wafer is recited before the acts of forming an

B

conductive layer and forming a gate by etching. Claim 11 recites a method of forming a structure for controlling current flow between a source and a drain region in a semiconductor device, wherein the semiconductor device is composed of a semiconductor wafer, an *insulating layer* disposed over the semiconductor layer, and a conductive layer disposed over the *insulating layer*, the method including the step of forming a gate having sidewalls exposing the conductive layer and some portion of the *insulating layer*. One skilled in the art would recognize that, according to claims 9 and 11, the gate is formed over the insulating layer. Oxide is known as the most common insulating layer in semiconductor devices.

Finally, one skilled in the art will understand that the layer of oxide 215 is necessary for the CMOS device to function. MOS transistor structures are defined by a source region and a drain region implanted in a substrate or an epitaxial layer on either side of a gate electrode, the gate electrode being insulated by a layer of gate oxide from a channel region in the substrate between the source and drain regions. The embodiment of the invention described in the application is a gate structure for a CMOS device. In Figures 2A-2D one skilled in the art will recognize that the layer 215 must be oxide to be consistent with what is known about gate structures in CMOS devices. A source region and a drain region are not shown because they are not necessary to a description of the embodiment of the invention which is, primarily, the selective spacer 210 that is deposited on the electrode 205 and not on the oxide layer 215.

Claims 26-31 and 36-41 are rejected under 35 USC § 112, second paragraph. The applicant respectfully traverses. In the above remarks the applicant pointed specifically to support in the specification for the term "a first layer of oxide".

Claims 23-31 are rejected under 35 USC § 112, second paragraph. The applicant respectfully traverses. The Examiner has indicated that the phrase "the feature having a surface" in the above-listed claims is not clear. The phrase "the feature having a surface" is found in independent claims 23, 26, and 30 and is further limited and identified as a sidewall of an electrode in the respective dependent claims 24, 28, and 31. The applicant respectfully submits that there is clear support in the specification and claims for the phrase.

B

Rejection under 35 USC §102

Claims 26 and 36 are rejected under 35 USC § 102(b) as being anticipated by Ho et al. (Ho, U.S. Patent No. 5,364,804). The applicant respectfully traverses.

Claim 26 recites, among other elements, a feature having a surface and a spacer comprising silicon nitride or an amorphous silicon film only on the surface of the feature. Ho discloses a spacer 26 of oxide on a gate electrode. Ho does not disclose the spacer comprising silicon nitride or an amorphous silicon film recited in claim 26. The applicant respectfully submits that Ho does not anticipate claim 26. Claim 36 also recites, among other elements, a spacer comprising silicon nitride or an amorphous silicon film. For the reasons stated above the applicant respectfully submits that Ho does not anticipate claim 36.

Rejection under 35 USC §103

Claims 23, 25-27, 29, 30, 36, 38, and 42 are rejected by the Examiner under 35 USC § 103(a) as being unpatentable over Ho in view of Manning (U.S. Patent No. 5,804,838). The applicant respectfully traverses.

Claim 23 recites, among other elements, an oxide layer, at least one feature over the oxide layer having a surface, and a spacer comprising silicon nitride or an amorphous silicon film covering the surface of the feature and terminating at a boundary with the oxide layer wherein the spacer is not in contact with the oxide layer. As mentioned above with respect to claim 26, Ho does not disclose such a spacer. Manning does not supply the elements missing in Ho. Manning discloses in Figure 10 silicon nitride spacers 48 and 50 on a feature 14 and in contact with a layer of oxide 13. Manning does not disclose the spacer recited in claim 23 that terminates at a boundary with an oxide layer. Therefore, even as combined, Ho and Manning do not disclose or suggest the elements recited in claim 23, or in claim 25 which is dependent on claim 23.

Claim 26 recites, among other elements, a feature over a first layer of oxide, the feature having a surface, and a spacer comprising silicon nitride or an amorphous silicon film only on the surface of the feature. For the reasons stated above with respect to claim 23, and the limitations in the claim, the applicant respectfully submits that claim 26 is not disclosed or suggested by the combination of Manning and Ho. In addition, the combination of Manning and

Ho does not disclose or suggest the limitations recited in claims 27 and 29 that are dependent on claim 26.

Claim 30 recites, among other elements, a feature over a first layer of oxide, the feature having a surface, and a spacer comprising silicon nitride or an amorphous silicon film only on the surface of the feature. For the reasons stated above with respect to claim 23, and the limitations in the claim, the applicant respectfully submits that claim 30 is not disclosed or suggested by the combination of Manning and Ho.

Claim 36 recites, among other elements, an electrode on a first layer of oxide, the electrode having sidewalls, and a spacer comprising silicon nitride or an amorphous silicon film deposited only on the sidewalls. For the reasons stated above with respect to claim 23, and the limitations in the claim, the applicant respectfully submits that claim 36 is not disclosed or suggested by the combination of Manning and Ho. In addition, the combination of Manning and Ho does not disclose or suggest the limitations recited in claim 38 that is dependent on claim 36.

Claim 42 recites a gate electrode comprising, among other elements, a feature having sidewalls and a selectively deposited spacer comprising silicon nitride or an amorphous silicon film, wherein the spacer is deposited only on the sidewalls of the feature. For the reasons stated above with respect to claim 23, and the limitations in the claim, the applicant respectfully submits that claim 42 is not disclosed or suggested by the combination of Manning and Ho.

Claims 24, 28, 31, 34, 37, 39-41, and 43 are rejected by the Examiner under 35 USC § 103(a) as being unpatentable over Ho et al. and Manning as applied to claims 23, 25-27, 29, 30, 32, 33, 35, 36, 38, and 42, above, and in further view of Gonzalez (U.S. Patent No. 5,608,249). The applicant respectfully traverses.

The Examiner cited Gonzalez for disclosing tungsten silicide in a gate. Gonzalez does not disclose any of the elements missing in Ho and Manning mentioned above. Therefore the applicant respectfully submits that the combination of Ho, Manning, and Gonzalez does not disclose or suggest the elements recited in claims 24, 28, 31, 34, 37, and 43 which are dependent on the claims discussed above.

Claim 39 recites, among other elements, a feature protruding from a first layer of oxide and having sidewalls, and a spacer comprising silicon nitride or an amorphous silicon film

B

selectively deposited only on the sidewalls of the feature. For the reasons stated above with respect to claim 23, and the limitations in the claim, the applicant respectfully submits that claim 39 is not disclosed or suggested by the combination of Manning, Ho, and Gonzalez. In addition, the combination of Manning, Ho, and Gonzalez does not disclose or suggest the limitations recited in claim 40 that is dependent on claim 39.

Claim 41 recites, among other elements, a feature protruding from a first layer of oxide and having sidewalls, and a silicon nitride spacer selectively deposited only on the sidewalls of the feature. For the reasons stated above with respect to claim 23, and the limitations in the claim, the applicant respectfully submits that claim 41 is not disclosed or suggested by the combination of Manning, Ho, and Gonzalez.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

KLAUS FLORIAN SCHUEGRAF ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6973

Date 4/9/99 By _____

Robert E. Mates
Reg. No. 35,271

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on April 9, 1999.

Jane E Brockschink
Name

Jane E Brockschink
Signature

B